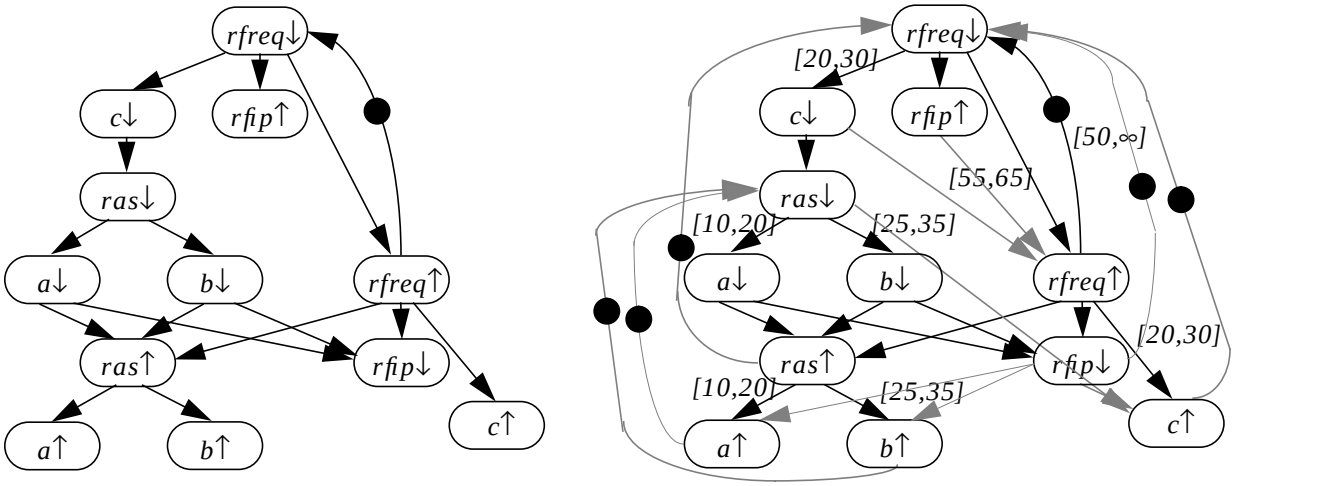


All unmarked solid rules have timing constraint *[0,2]*.
All dashed rules have timing constraint *[0,0]*.

(a) (b)

Figure 9: Constraint graph specification for the *refresh* cycle of the DRAM controller: (a) initial specification and (b) strongly connected specification.

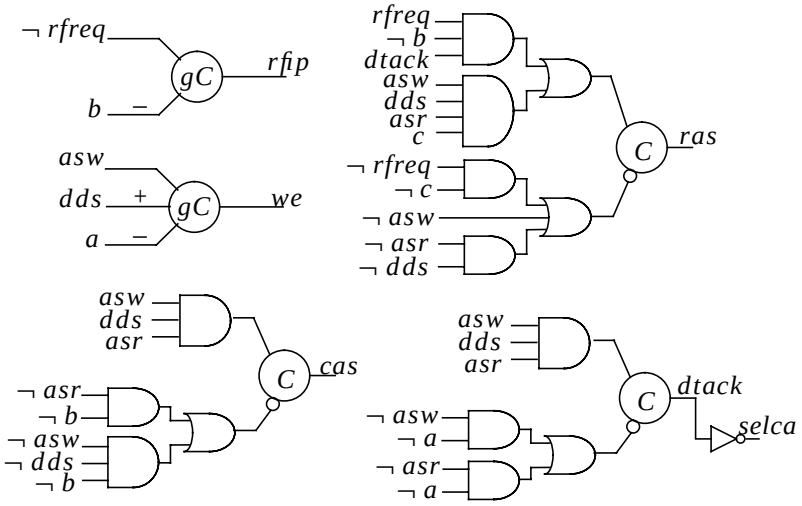


Figure 10: Timed circuit implementation of the DRAM controller.

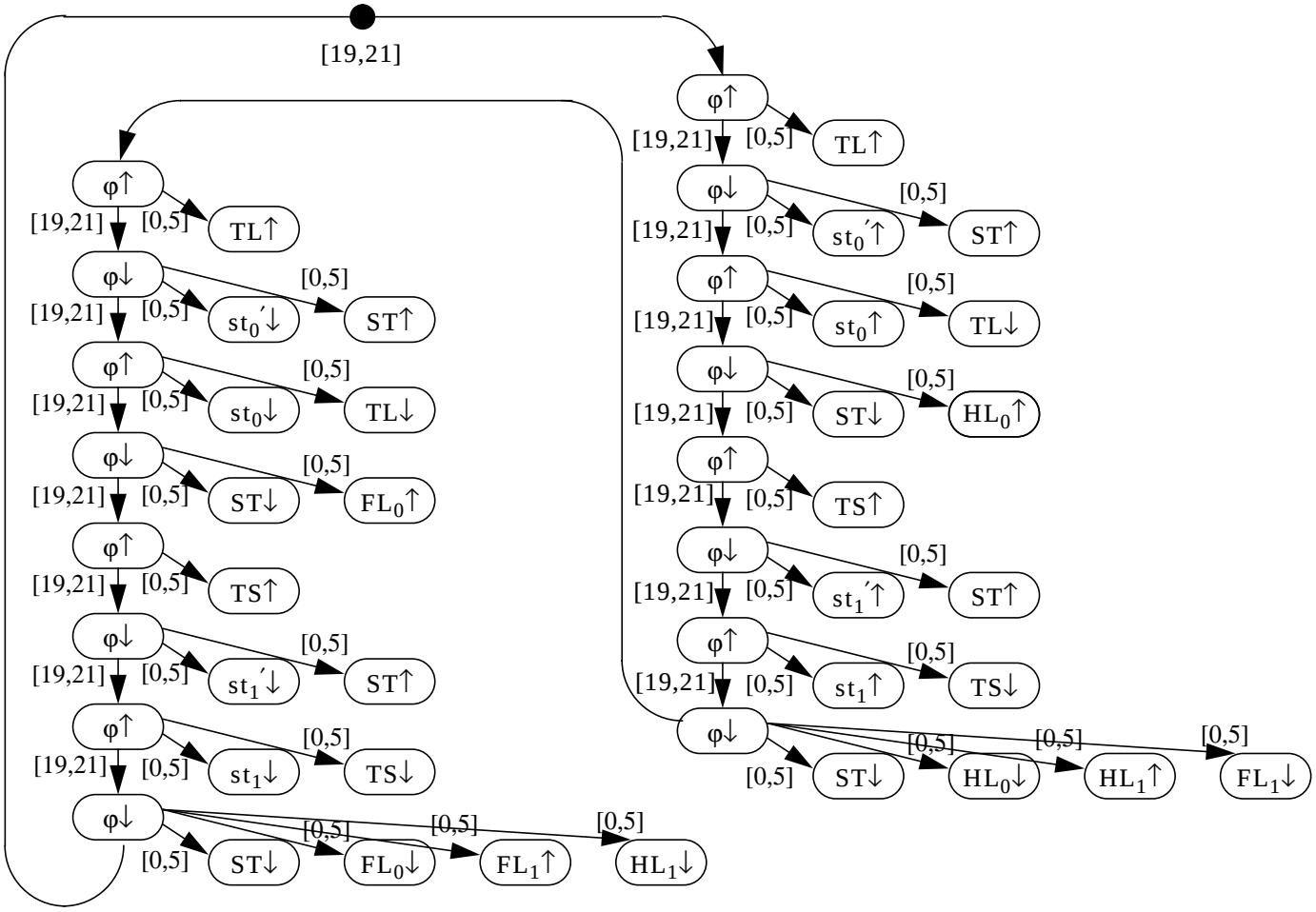


Figure 7: Cyclic constraint graph specification for traffic light controller.

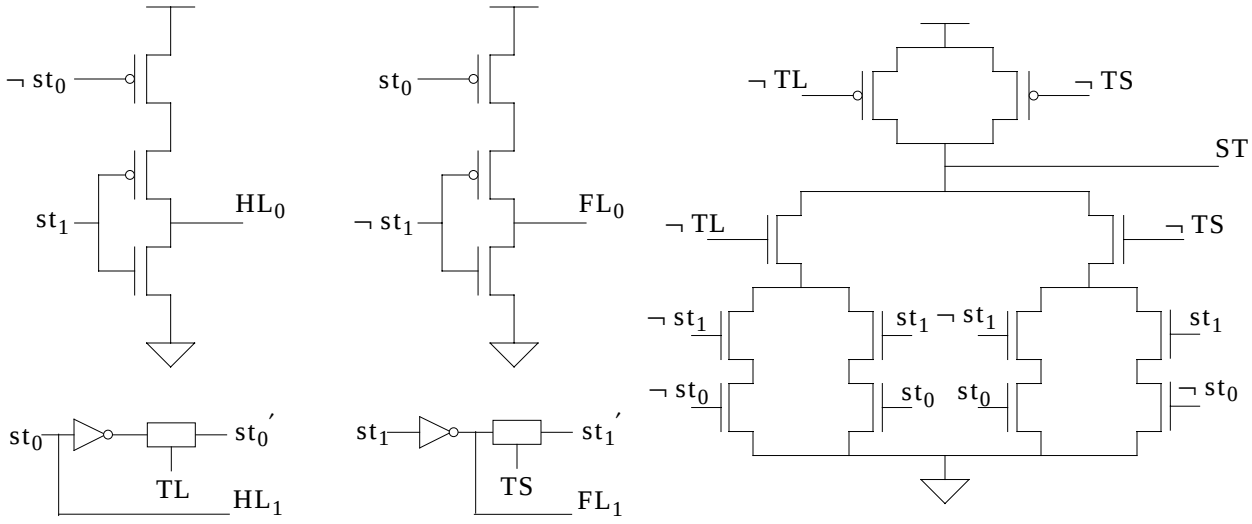


Figure 8: Timed circuit implementation of the traffic light controller.

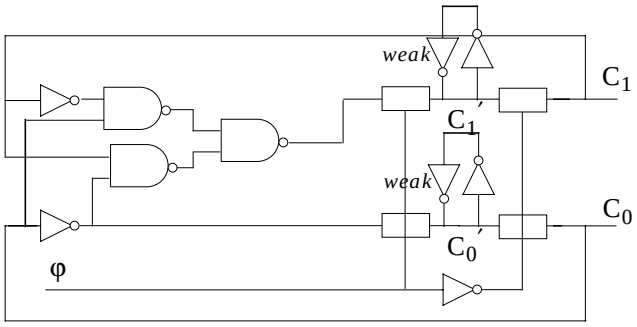
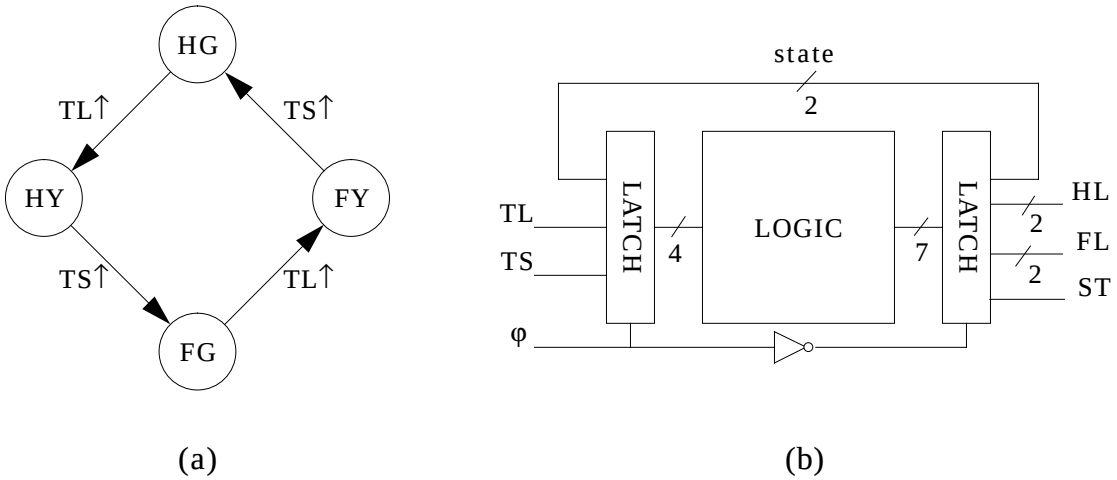


Figure 5: SIS implementations of a two-bit synchronous counter.



(a) (b)

Figure 6: Determininistic version of Mead and Conway's traffic light controller: (a) state diagram and (b) block diagram.

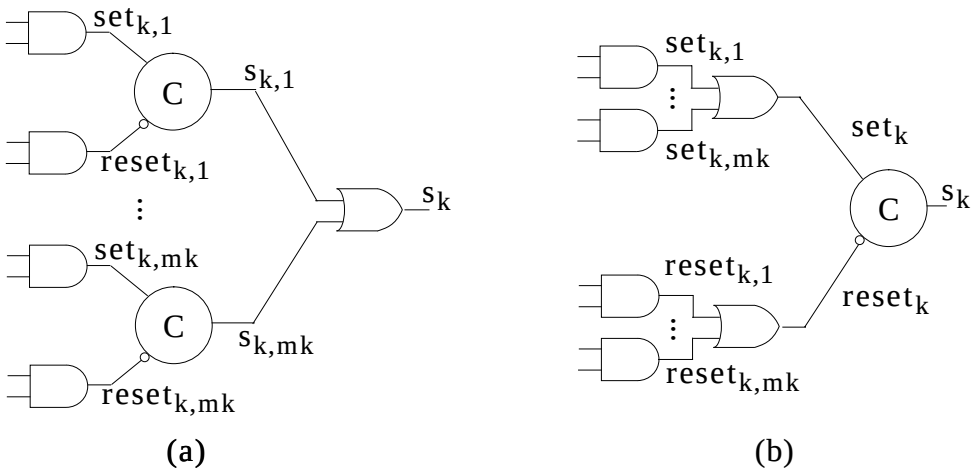


Figure 3: Choice of gate structure for signals which occur multiple times in a cycle: (a) merge structure and (b) complex gate structure

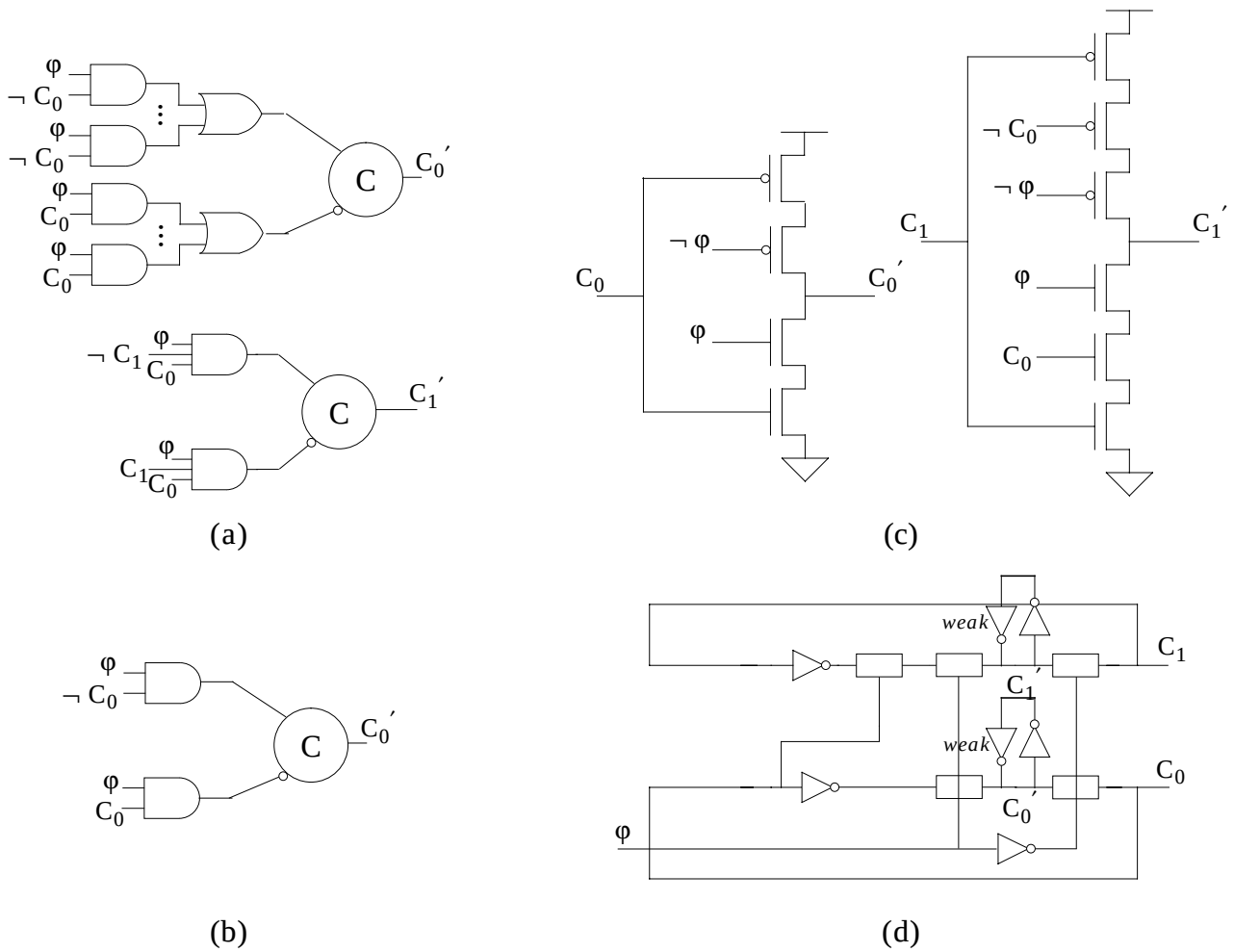


Figure 4: Timed circuit implementation of two-bit synchronous counter: (a) complex-gate structure, (b) simplified C_0', (c) transistor-level, and (d) using latches.

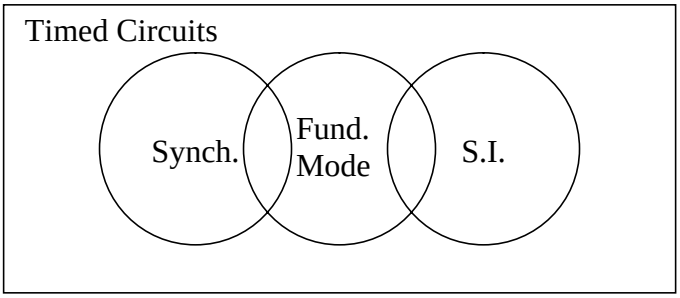


Figure 1: Summary of relationships between system timing models.

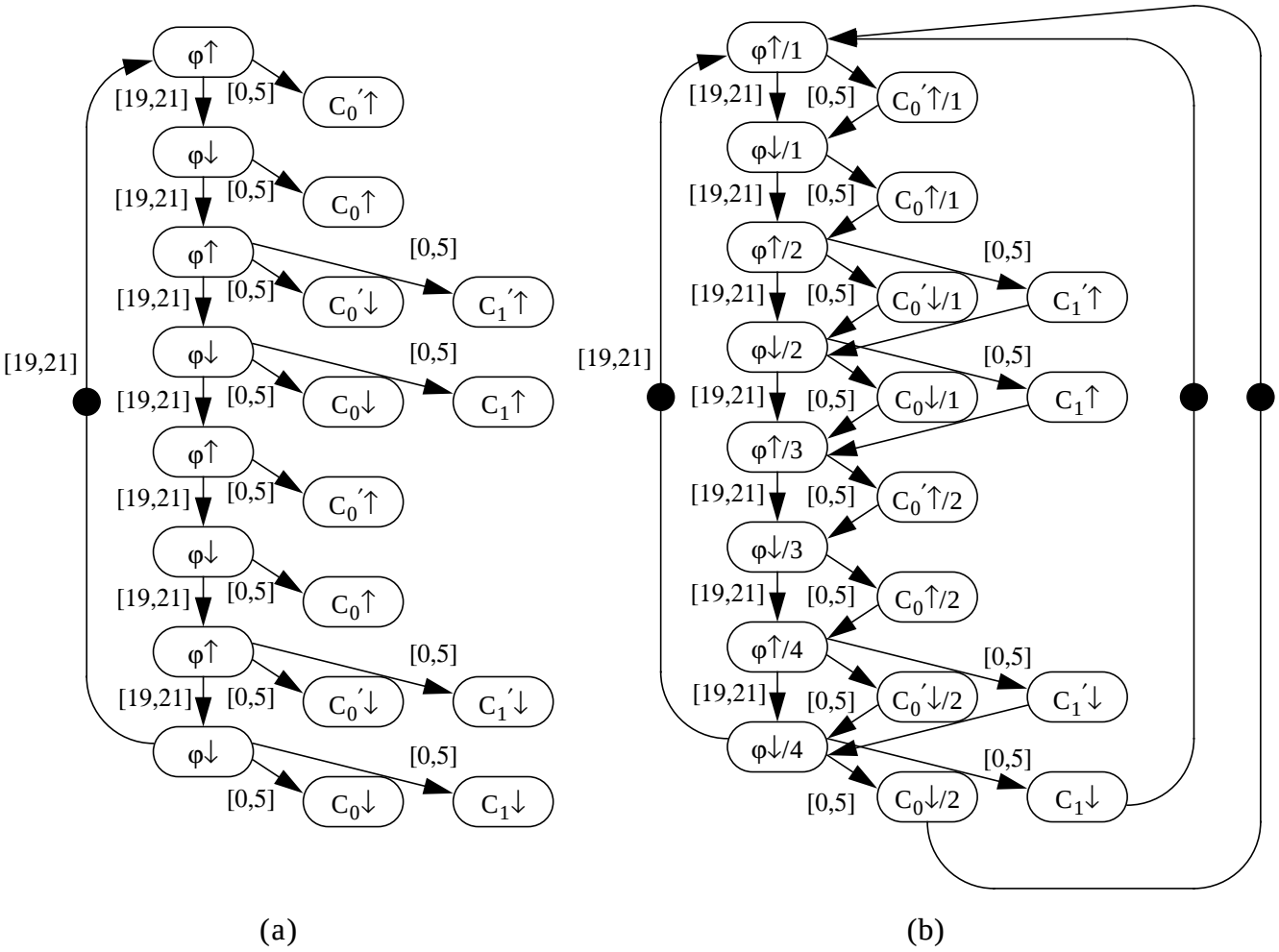


Figure 2: The constraint graph specification for a two-bit synchronous counter: (a) initial specification and (b) final specification.