Design-for-Current Testability (DFCT) for Dynamic CMOS Logic

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CRC Technical Report No. 94-13

(CSL TR No. 94-643)

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Abstract

The applicability of quiescent current monitoring (IDDQ testing) to dynamic logic is discussed here. IDDQ is very useful in detecting some defects that can escape functional and delay tests, however, we show that some defects in domino logic cannot be detected by either voltage or current measurements. A design-for-current-testability (DFCT) modification for dynamic logic is presented and shown to enable detection of these defects. The DFCT circuitry is designed with a negligible performance impact during normal operation. This is particularly important since the main reason for using dynamic logic is because of its speed.

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1. INTRODUCTION

Dynamic circuits are used in modern VLSI designs where both high speed operation and high packing density are required [Suzuki94][Undy94][Yeung94]. Testing of dynamic logic has been addressed in several papers [Singh88][Wunderlich86][Ling87][Jha90a-c] [Tong90]. Wunderlich [Wunderlich86] and Singh [Singh88] showed that stuck-open faults in domino logic are easier to detect than stuck-open faults in static CMOS circuits. This is because stuck-open faults are detected by applying two pattern tests; the precharge phase in dynamic logic provides one pattern, and the evaluation phase provides the other pattern. Therefore, any single input vector in dynamic logic is inherently applied as a two pattern test. Because of this property, delay test generation is also easier for dynamic logic [McGeer91][Bruni92]. Robust path delay fault testability is also guaranteed if any given path is staticly sensitizable [McGeer91].

It is believed that quiescent supply current monitoring (IDDQ testing) can detect some defects that cannot be detected by functional tests [Maxwell92][Gayle93]. Other advantages of IDDQ testing include simpler test pattern generation (no fault propagation required) and reduced test set sizes compared to functional tests [Fritzemeier90]. Stuck-open faults, excessive leakage, shorts and bridging faults in dynamic circuits are shown to be detectable using IDDQ testing [Jacomino89][Renovell93]. Vandris showed that stuck-on faults can always be detected by either functional or IDDQ tests [Vandris91]. However, these papers assumed that we have full controllability on the inputs of a dynamic logic gate, and those inputs can be held constant during the supply current measurement time. This is not always true when the inputs to a dynamic logic gate are connected to the output of another dynamic logic gate, since dynamic nodes may lose their stored charge if the dynamic circuit is not clocked at a high frequency. A CMOS microcomputer IC with dynamic circuitry was subject to IDDQ testing and reported in [Horning87]. Their results suggested that IDDQ can be performed at 50kHz without concerns of losing storage charge in dynamic nodes. Other IDDQ problems for dynamic CMOS circuits are discussed in [Lee92], such as undetectable internal bridges, charge sharing, and multiple bridging faults. These problems are revisited in Sec. 3 with our proposed solution.

A unique failure mode, called a *Stationary Fault,* is presented in this paper. A stationary fault occurs when the output of a faulty gate makes a correct transition and then settles to an incorrect steady-state value [Ma92]. Stationary faults in dynamic circuits are caused by either a short or a floating gate. Shorts and floating gates are detectable by IDDQ testing under certain conditions [Champac93]. However, because of the nature of dynamic circuits, some bridging faults are undetectable by IDDQ tests. We will show that a bleeder circuit can be used to improve the bridging fault coverage of IDDQ tests in dynamic circuits. The disadvantage of adding a bleeder circuit is its large performance overhead. It order to minimize the performance impact, a design-for-current-testability (DFCT) scheme is proposed. We will focus on *domino logic* [Weste93]; however, the results are applicable to any precharged dynamic logic circuitry. The rest of this paper is organized as follows. A brief discussion of domino logic and its IDDQ-relevant properties is given in Sec. 2. Stationary faults in dynamic circuits are discussed in Sec. 3. Section 4 presents the issues in applying IDDQ tests to domino logic, and DFCT solutions for these issues are proposed in Sec. 5.

2. DOMINO LOGIC

A domino logic AND gate is shown in Fig. 1. The gate function is provided by NMOS transistors MA and MB. The operation of a domino logic is split into two phases: the *precharge phase,* when the clock input Clk is 0, and the *evaluation phase*, when the Clk is high. During the precharge phase, Z is disconnected from ground, since transistor MN is off. PMOS transistor MP is on during precharge, and node Z is charged to V_{DD}. Therefore, the output Out is always 0 during the precharge phase. During the evaluation phase, MP turns off and MN turns on; node Z will either discharge to 0 if both A and B are high, or stay at V_{DD} otherwise. If Z is discharged, Out will rise to V_{DD}, otherwise it will stay at 0. Notice that if the dynamic node Z is not discharged through the MA, MB and MN, there is still a leakage current that discharges Z slowly. If the circuit is not clocked fast enough to precharge Z again, a transition from 0 to V_{DD} on the output may occur. The Domino AND gate was simulated using SPICE to search for the minimum clocking frequency. The results of the simulations are given in Sec. 3.

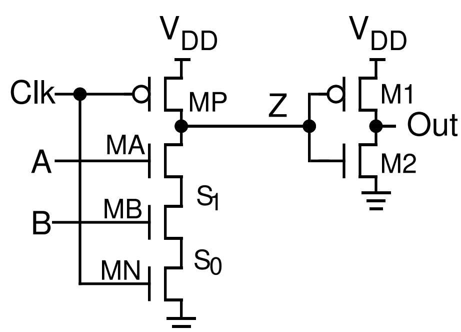

Figure 1. Domino AND Gate

Typically, several stages of domino gates are connected together to form a combinational logic block [Kernhoff90]. The dynamic node in each gate of the combinational block is charged to V_{DD} during the precharge phase. During the evaluation phase, the output of one level of domino gates may switch from 0 to V_{DD}, which is also the input to the next stage. This next stage can also make a rising transition, triggering the following stage. Notice that during evaluation, the dynamic node can only discharge, it cannot be recharged again. The rising transitions propagate from one level to another until all nodes are stable except for leakage current.

3. CMOS STATIONARY FAULTS

It is believed that stuck-at faults do not accurately model real defects in static CMOS circuits [Fritzemeier91]. Switch level fault models (stuck-open, stuck-on, bridging) and transistor level fault models (shorts, opens) are used for more accurate representations of defects [Abraham86]. These models are also used for modeling defects in dynamic CMOS [Rajsuman92][Jha90a].

The output of a defective BiCMOS gate can make a correct transition and then settle to an incorrect steady-state value [Ma92]. This faulty behavior, called a *stationary fault*, can escape functional and delay tests.

Stationary faults can occur in precharged circuits as follows. Consider the domino AND gate in Fig. 1. Assume that there is excessive leakage from source-to-drain of MB. This leakage can be caused by either a gate-oxide short [Hawkins85] or a floating gate [Champac94]. During the precharge phase, node Z is charged to V_{DD}. When Clk becomes high, the charge on Z will leak through the source-drain junction of MB assuming a defect in MB, if MA is on (A is high). Depending on the leakage current, the output Out may or may not switch before the next precharge cycle. The amount of leakage current depends on the defect size, and the surrounding layers in the case of a floating gate [Champac94]. If the leakage current is large enough such that the output Out switches before the next precharge cycle, a stationary fault occurs. It is very conceivable that such a defect will escape a functional test and then fail in the field because of different operating conditions.

To illustrate this, the circuits shown in Fig. 2 and Fig. 4 have been laid out using Magic [Mayo90] with MOSIS Scalable CMOS design rules, and SPICE decks have been extracted with HP 1.0μ n-well technology. Each of the two circuits contain a faulty domino AND gate, whose inputs A and B are driven by domino buffers, and output Out is buffered with a domino buffer. Two simulation sequences were carried out using HSPICE; a source-to-drain short was injected into MB in the first simulation sequence (Fig. 2), and an intermediate voltage level was held on B in the second simulation sequence (Fig. 4).

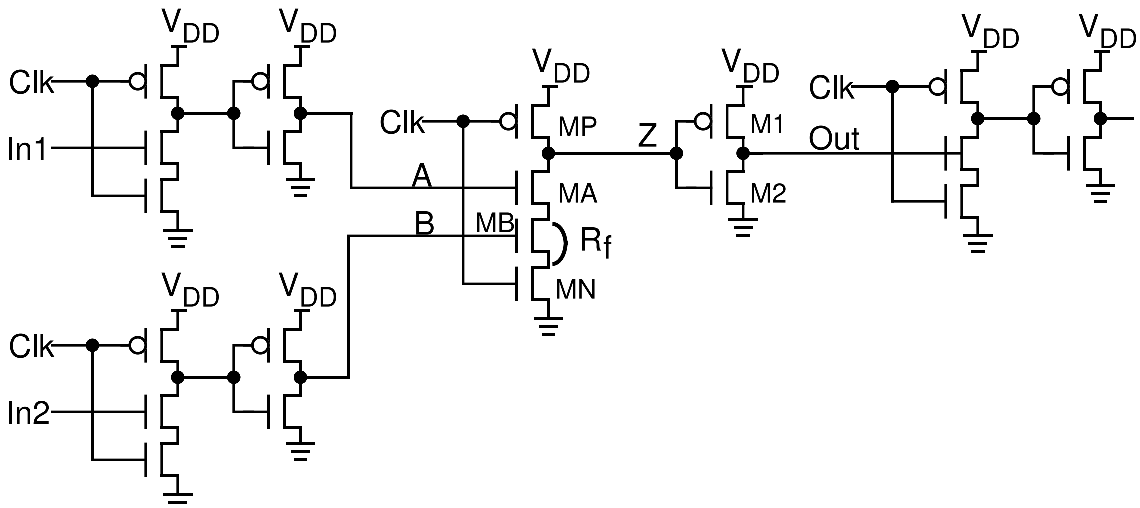

Figure 2. Simulated Domino Logic Circuit: With source-drain short R_f on MB

The short resistance value R_f in Fig. 2 was varied from 0 to 8kΩ. These resistance values covers the range of resistance values measured in real defects [Hawkins85]. Inputs In1 and In2 were held at V_{DD} and 0, respectively. The Clk input was changed from 0 (precharge) to V_{DD} (evaluate). Charge is stored on node Z during the precharge phase, and leaks to ground through the source-to-drain short during evaluation. When the voltage on Z drops below the threshold of the output inverter (M1 and M2), a faulty rising transition occurs on the output of the AND gate Out. For each short resistance R_f, the *leakage time*, the time from the Clk transition to the faulty Out transition, was measured. Figure 3 shows the relationship between the short resistance R_f and the leakage time. The leakage time defines the period where the output is held at a correct logic value. After this period, a faulty transition occurs, and the output switches to an incorrect logic value. We also measured the rising propagation time from Clk to Out (t_{plh}) for a fault free domino AND gate with both inputs In1 and In2 held at V_{DD}. This rising propagation time is the minimum time required for evaluation of a 2 input AND gate, which is measured at 0.492ns (solid horizontal line in Fig. 3). If the circuit was tested at-speed, Clk may be driven such that the evaluation time allocated for the AND gate is 0.492ns. However, this evaluation period is shorter than the leakage time for any R_f > 1kΩ, which means that shorts with these resistance values will escape at-speed tests.

In Fig. 4, V_B was varied from 0 to V_{DD} to model a floating gate with different gate voltages. For each voltage value, Clk was changed from 0 to V_{DD} with In1 held at V_{DD}, and the leakage time was measured. Figure 5 shows the relationship between the voltage on the floating gate and the leakage time. Notice that a floating gate with a voltage less than 1/2 V_{DD} is detectable with an functional test by applying V_{DD} on both In1 and In2, where the output Out of a faulty gate takes more than 0.60ns to switch to the correct high value, while the output Out rises in 0.492ns in a fault free gate. On the other hand, if the voltage on the floating gate is greater than 1/2 V_{DD}, we can detect this floating gate by applying V_{DD} on In1 and GND on In2. A faulty transition can be observed on the output of a faulty gate, whereas no transition will occur in a fault-free gate. Practically, the voltage on a floating gate is not constant, but depends on the voltage levels of surrounding layers and the coupling between these layers and the floating gate [Renovell93]. Therefore, it is possible that a floating gate would escape any functional tests.

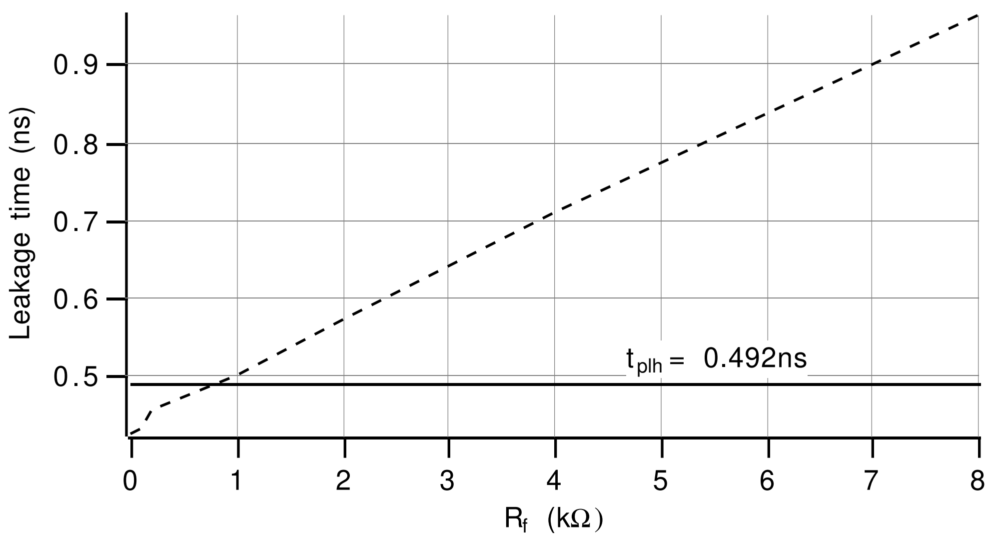

Figure 3. Leakage time for source-drain short on MB

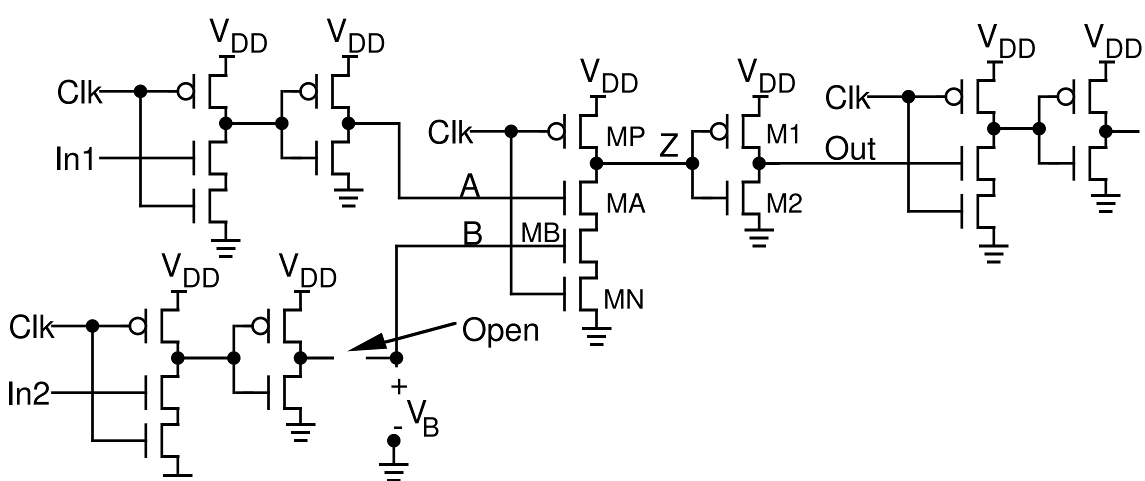

Figure 4. Simulated Domino Logic Circuit: Floating Gate on MB

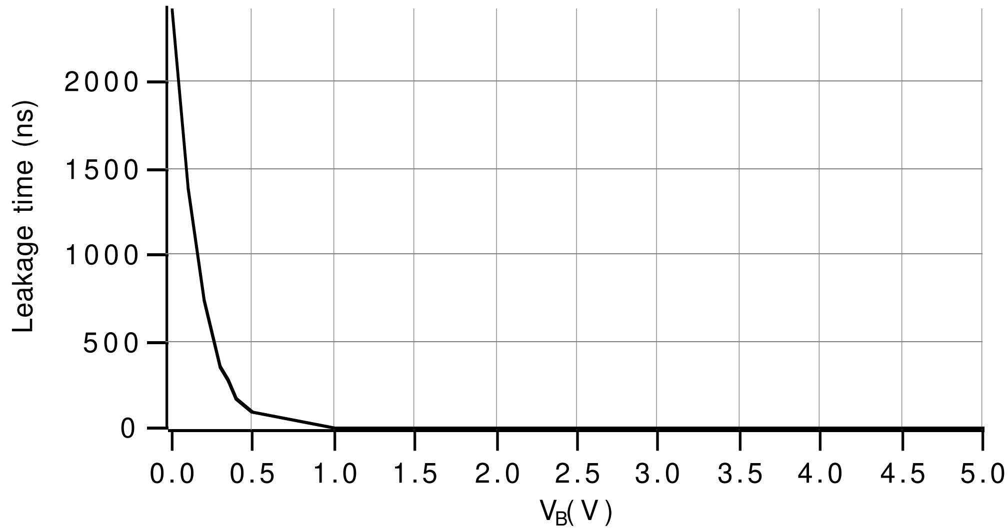

Figure 5a. Leakage time for floating gate on MB (V_B between 0 and 5V)

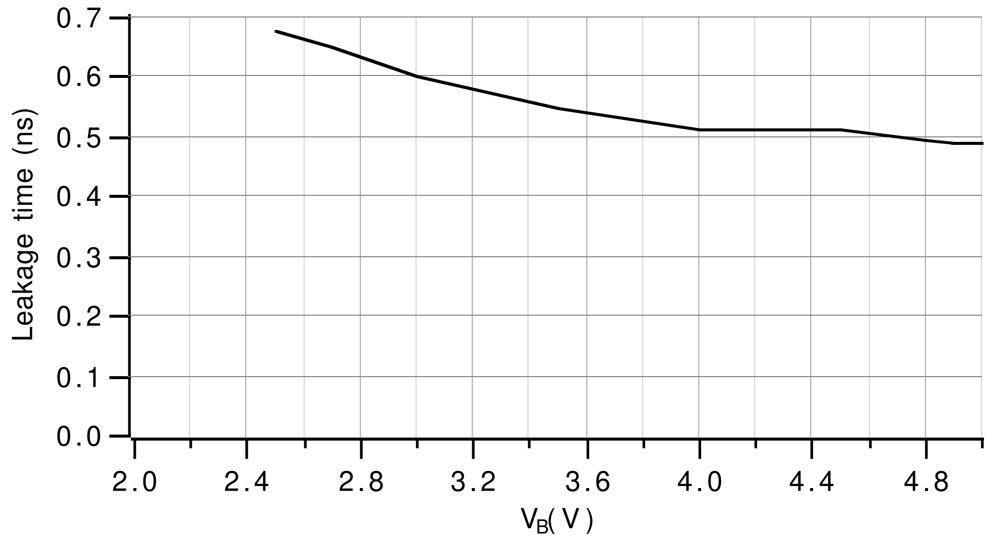

Figure 5b. Leakage time for floating gate on MB (V_B between 2.5 and 5V)

4. IDDQ TESTING OF DOMINO LOGIC

Several issues must be addressed before IDDQ testing can be reliably applied to domino circuits. These issues include fault coverage and undetectable bridges, minimum operating frequency for dynamic circuits, excessive leakage current induced by intermediate voltage levels, and excessive leakage current due to charge sharing. These issues are due to limitations in the current sensing devices and the dynamic logic nature of the circuitry.

4.1 Fault Coverage

A major question in supply current monitoring tests is how to measure the effectiveness of the test. Since supply current monitoring is believed to be able to detect most bridging faults and internal shorts, several IDDQ studies used these faults to generate IDDQ test vectors or fault grade their IDDQ test vectors [Nigh90][Lee92][Aitken93][Renovell93].

To evaluate the detectability of shorts in domino logic gates, Renovell [Renovell93] classified the nodes in a domino gate into two classes: a class that contains V_{DD}, ground, Clk and primary inputs, and another class that contains all internal nodes. For the domino AND gate shown in Fig. 1, class 1 contains nodes V_{DD}, ground, Clk, A and B, and class 2 contains nodes Z, S_0, and S_1. Renovell showed that shorts between class 1 nodes and class 1 or class 2 nodes are IDDQ testable, whereas all shorts between two class 1 nodes are not IDDQ testable [Renovell93]. He assumed that any input combination can be applied at any phase of the clock in a domino circuit. This is not true during the precharge phase where all dynamic nodes are charged high, and the output of each domino gate is 0. In this case, some shorts between class 1 and class 2 are untestable. For example, consider the short between S_1 and ground in Fig. 6. According to [Renovell93], this short is detectable since ground is a class 1 node. This is only true if we apply a high voltage on A, and turn MP on. However, to turn MP on, Clk must be 0, and the output of all domino gates are 0. If A is driven by another domino gate, then the high voltage required on A to detect the S_1-to-ground short cannot be applied. Table 1 summarizes the difference between Renovell's results, where gate inputs are fully controllable, and our results, when the gate inputs are driven by another domino gate. For each bridging fault, Table 1 lists the detectability of the fault by an IDDQ test, and whether the fault is detectable during precharge or evaluation phase.

From Table 1, we conclude that several bridging faults in dynamic circuits cannot be detected by IDDQ tests, especially when the inputs to the dynamic circuits are not fully controllable.

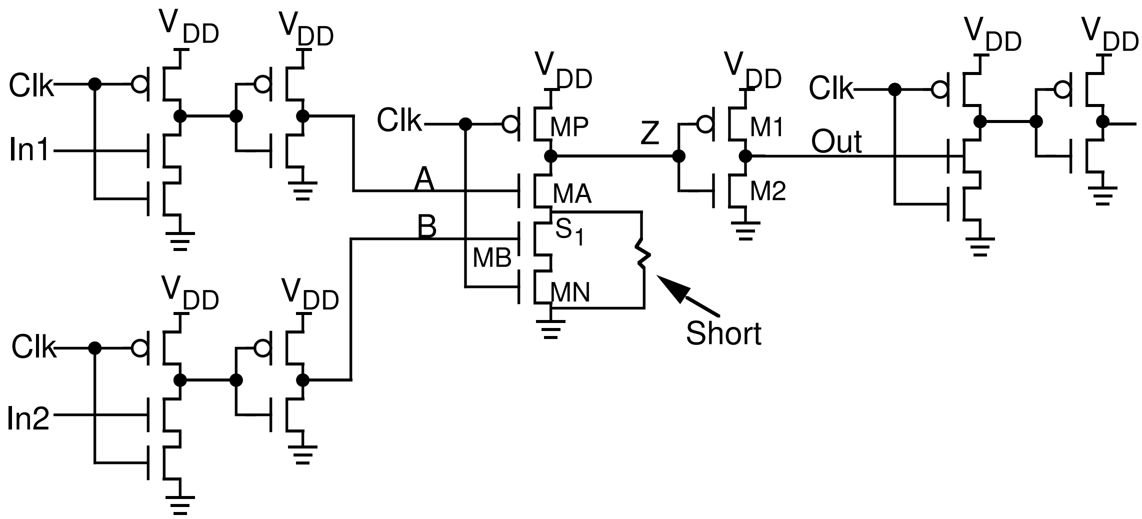

Figure 6. S_1-ground bridge

Table 1 Bridge Detectability by IDDQ Tests

	Controllable Inputs [Renovell93]		Uncontrollable Inputs	
Bridge	Precharge Detection	Evaluation Detection	Precharge Detection	Evaluate Detection
VDD/GND	Yes	Yes	Yes	Yes
VDD/Clk	Yes	No	Yes	No
GND/Clk	No	Yes	No	Yes
A/B	Yes	Yes	No	Yes
A/Z, B/Z			Yes	Yes
A/S0, B/S0	Yes	Yes	No	Yes
A/S1, B/S1			No	Yes
Z/S0, Z/S0, S1/S0	No	No	No	No
VDD/A, VDD/B	Yes	Yes	Yes	Yes
VDD/Z VDD/S0 VDD/S1	No	Yes	No	Yes
GND/A GND/B	Yes	Yes	No	Yes
GND/Z			Yes	
GND/S0	Yes	No	No	No
GND/S1			No	
Clk/A Clk/B	Yes	Yes	No	Yes

Clk/Z Clk/S0 Clk/S1	Yes	Yes	Yes No No	Yes

4.2 Minimum Operating Frequency

Quiescent supply current are typically measured at 10 to 100kHz by external current measurement devices [Hawkins89]. Measurements at higher speeds (a few MHz) requires special instrumentation to reduce the long transient disturbances introduced by test pin impedance. Dynamic nodes may not maintain their storage charge at such low frequencies, especially in submicron technologies, where subthreshold currents can be fairly large [Muller86]. If dynamic nodes are unable to maintain their charge during the measurement time, two problems can occur: the dynamic nodes may switch before any measurement is made, or the degraded voltage levels may induce more leakage current in the gate driven by the dynamic nodes.

The first problem leads to lower fault coverage because some test vectors cannot be applied. The leakage time defines the period when the correct logic value is preserved. Beyond the leakage time, the output logic value is lost. For the domino AND gate shown in Fig. 1, with A and B held at V_{DD} and ground respectively, the leakage time is 2.42µs. This means that current measurements should be made at a minimum frequency of 400kHz (1/2.42µs) to ensure that sufficient input vectors are applied to the domino AND gate.

The second problem, which is more severe than the first problem is discussed in the next section.

4.3 Intermediate Voltage Levels

When the charge on dynamic node Z drops below the threshold of M1 (Fig. 1), both M1 and M2 are on, and therefore a large current may flow from V_{DD} to ground. This current may be large enough to mask out any excessive current caused by real defects. Horning conjectured from his experiments on a microcomputer chip that contains dynamic circuitry that the voltage drops on dynamic nodes were not severe enough to cause excessive current to flow [Horning87]. However, in modern deep submicron technologies, the subthreshold current may be significant [Muller86] and storage capacitances are minimized for higher switching speed. A larger subthreshold current means that the leakage current is much higher at very low gate voltages, while smaller storage capacitances mean that less charge is stored, and less current is required to discharge storage nodes, which means that the leakage time is much shorter in submicron technologies.

Based on our simulations of the circuit shown in Fig. 4, the leakage current increased by three orders of magnitude (approximately from 50 nA to 50μA) within the first microsecond. This means that for a few hundred domino gates, the leakage current could increase to the milliamp range when a 1MHz current sensing tester was used, and even higher when a slower current sensing tester was used, which may mask out excessive current caused by real defects.

4.4 Charge Sharing

Charge sharing can degrade the voltage level on dynamic nodes. To illustrate this, consider the domino AND gate in Fig. 1. Assume that A and B are connected to ground and V_{DD} respectively in the first evaluation cycle. Therefore, node S_1 is discharged to ground. After the next precharge cycle, which charges node Z to V_{DD}, assume that A and B switch to V_{DD} and ground, respectively. Some of the charge stored on node Z will flow to node S_1, until both node Z and S_1 have the same voltage level. The capacitance on node Z should be designed to be larger than the capacitance on node S_1 to make sure that node Z maintains its logic level even if charge sharing occurs. However, this does not prevent the voltage level on node Z from dropping below the threshold voltage for M1, which leads to large current flow through M1 and M2. This large current may invalidate an IDDQ test.

5. DESIGN FOR CURRENT TESTABILITY FOR DOMINO LOGIC

The problems raised in Sec. 4 can be avoided by using the bleeder circuit shown in Fig. 7. The same structure of the bleeder circuit is found in [Weste93]. The PMOS transistor M3 is a weak transistor that prevents node Z from dropping below V_{DD} whenever the output Out is 0. If Z is pulled down low, the output Out switches to V_{DD}, and M3 is turned off. The size of the AND gate with the bleeder circuit is the same as the gate without the bleeder circuit (22.5μm x 16μm), since we can fit the extra PMOS gate in the free space left beside the other two PMOS transistors M1 and MP. This extra M3 transistor solves the IDDQ issues as follows:

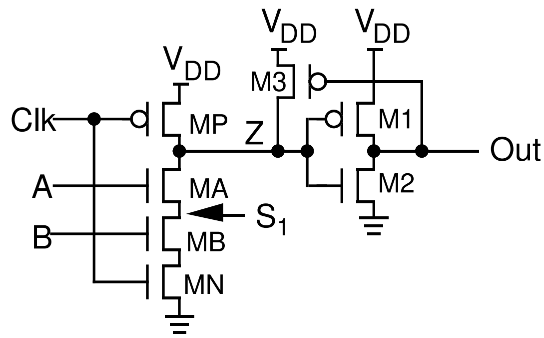

Figure 7. Domino AND Gate with bleeder circuit

1. Fault Coverage:

The bridging fault between S_1 and ground can be detected by either a voltage or a current test by applying V_{DD} and ground on A and B respectively. If the bridge resistance is low, the output can switch in a relatively short time, and voltage tests (functional tests) can detect this fault. In this case, the fault free output is 0, while the faulty output is V_{DD}. If the bridge resistance is high, the output may take a long time to switch, which means that the output is held at 0 for a long time, and transistor M3 is on. In this case, transistor M3 provides a current path between V_{DD} to ground through the bridge, and hence the bridge can be detected by supply current monitoring. Bridges between two class 1 nodes are also detectable by either voltage or current tests by the same argument. With the bleeder circuit shown in Fig. 7, many undetectable shorts become detectable or potentially detectable.

In general, the bleeder circuit will try to maintain the value of Z at V_{DD}. This means that the leakage time for given short with resistance R_f in a domino gate with a bleeder circuit is longer than the leakage time for the same short in a gate without a bleeder circuit. Therefore, we need to run a slower test to detect the same short in a bleeder circuit. The bleeder circuit increases the range of short resistances that are detectable by current tests, but decreases the range of short resistances that are detectable by boolean tests.

2. Minimum Operating Frequency

Since the output of each domino gate is held static during the evaluation phase, there is no restriction on minimum operating frequency.

3. Leakage Currents

The bleeder circuit ensures that the dynamic nodes are either held at V_{DD} or ground in a fault-free domino gate, hence no excessive leakage current will occur in the output inverter M1 and M2.

4. Charge Sharing

Charge lost from dynamic node Z due to charge sharing is restored rapidly by the bleeder circuit, hence charge sharing will not lead to excessive leakage current.

Notice that M3 opposes Z from discharging until Out switches high, hence the rise time for Out is higher. Our simulation shows that t_{plh} increases by approximately 24% (from 0.492ns to 0.612ns) by adding M3. This performance penalty may be too large, since the main purpose of using dynamic logic is because of its high switching speed. Furthermore, if we need higher IDDQ detectability, M3 should be sized larger so that more current can flow through the bridge. Increasing the size of M3 will increase the load capacitance on Out, and oppose Z from discharging fast during normal operation, which translates to more performance degradation in the circuit.

To solve this problem, we propose the DFCT domino circuit shown in Fig. 8, where M3 is turned off during normal operation (ITEST=0) and turned on during IDDQ testing (ITEST=1). Increasing the size of M3 in this case does not degrade the performance of the circuit. Our SPICE simulations showed that t_{plh} increases by 1ps only (from 0.492ns to 0.493ns) when ITEST=0. When ITEST=1, IDDQ can reach as high as 1mA in presence of a floating gate, compared to a few microamps for the same defect in a pure domino gate (Fig. 1). The size of the DFCT domino AND gate shown in Fig. 8 is 20% larger (22.5µm x 20µm) than the domino AND gate shown in Fig. 1. The area penalty is much smaller for a typical complex domino gate.

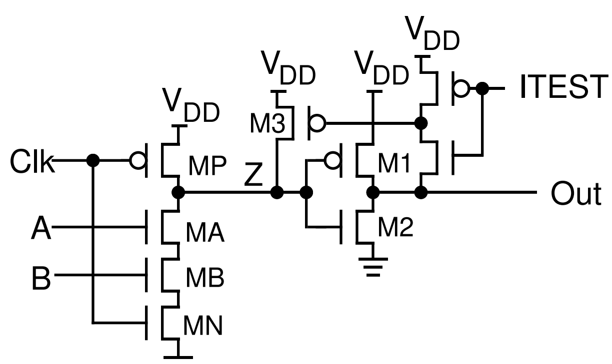

Figure 8. Domino AND Gate with DFCT circuitry

The DFCT domino circuit also solves the problem of the smaller range of short resistances detectable by boolean tests for domino gates with bleeder circuit. During a boolean test, the bleeder circuit in the DFCT domino circuit can be turned off by applying ITEST=0 to decrease the leakage time. In this case, the leakage times are almost identical to those shown in Fig. 3, which means that the range of short resistances that are detectable by boolean tests in a DFCT domino circuit is the same as in a normal domino circuit without the bleeder circuit.

6. CONCLUSIONS

Stringent test procedures must be applied to dynamic circuits to ensure adequate quality levels, since dynamic circuits are used in high speed components. Some defects may be untestable by at-speed or delay tests, although these defects are likely to produce errors in the field. These defects are detectable by IDDQ tests, however, special care is needed when we apply IDDQ testing on dynamic circuits. An inappropriate current measurement may fail a perfectly reliable dynamic circuit, and an inadequate current measurement setup may pass some defective dynamic circuits. To achieve high fault coverage of IDDQ tests of dynamic circuits, some design-for-testability circuitry must be added. This is because of the dynamic nature of some nodes; even if a bridge occurs from a power supply or ground to the dynamic node, there is may be no current path between power supply and ground. The design-for-testability circuitry must be able to detect these bridges, while keeping the performance overhead at a minimum.

ACKNOWLEDGMENTS

This work was supported in part by the Innovative Science and Technology Office of the Strategic Defense Initiative Organization and administered through the Office of Naval Research under Contract No. N00014-92-J-1782, and by the National Science Foundation under Grant No. MIP-9107760.

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